

Fig. 1: Block diagram for the transmitter of the proposed system
 (a) Transmitter structure
 (b) Data structure, before and after block spreading module

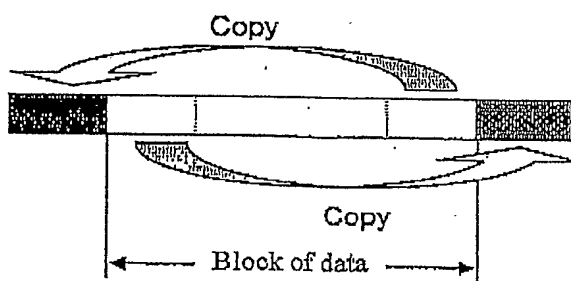


Fig. 2: Details of insertion of cyclic extension

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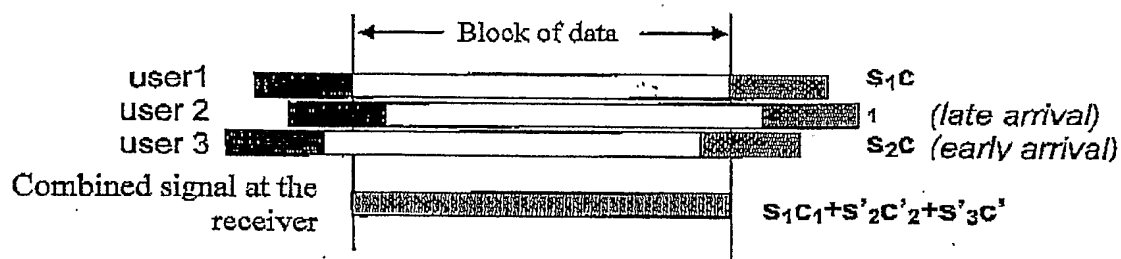


Fig. 3: The combined received signal for cyclic extended asynchronous transmission for ideal channel

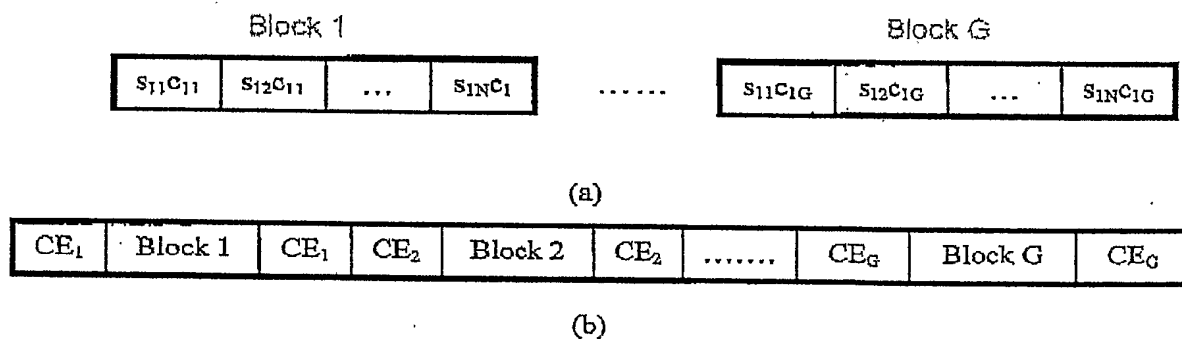


Fig. 4: The packet structure before and after the insertion of cyclic extension
(CE1 is cyclic prefix and CE2 is cyclic postfix)

(a) Block structure after parallel-to-serial conversion

(b) One TP spreading module after the insertion of cyclic prefix

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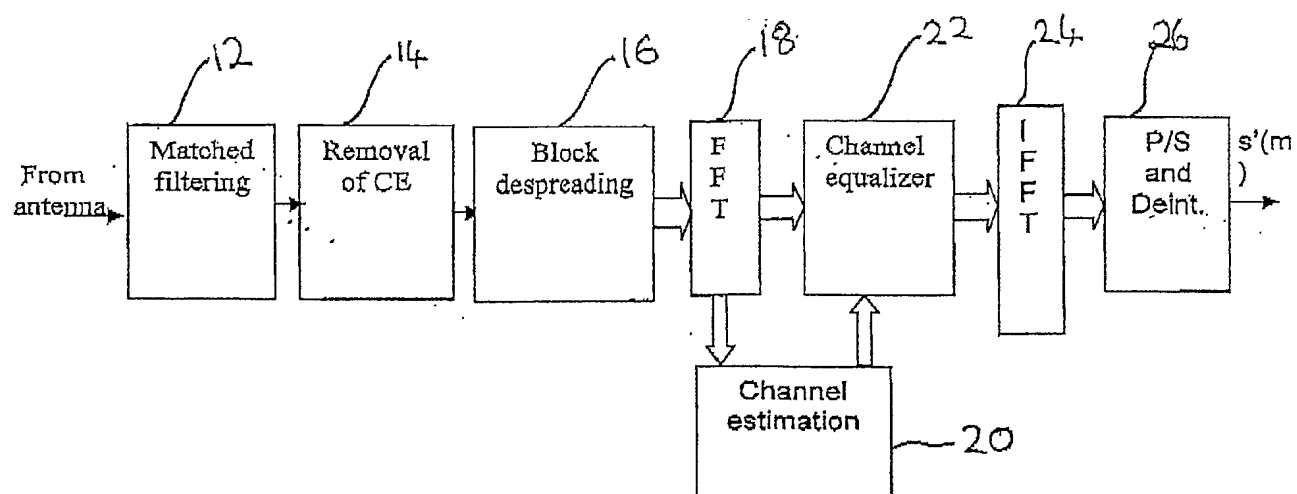
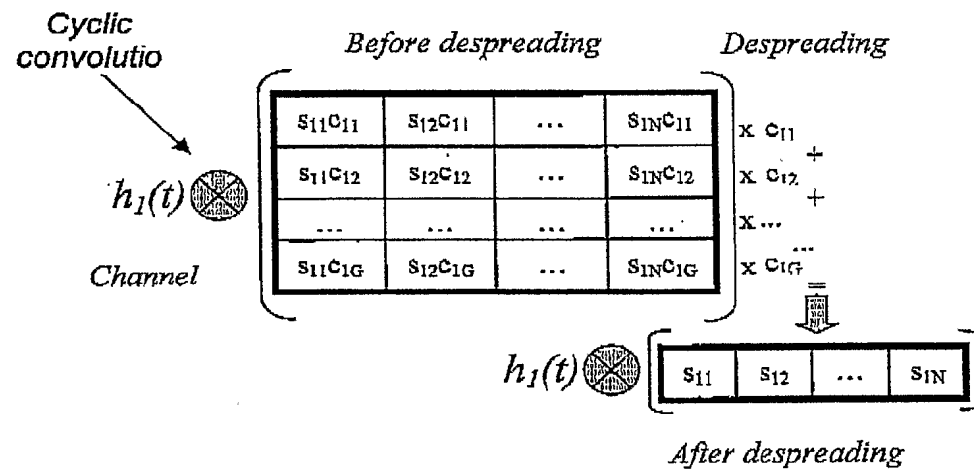


Fig. 5: Block diagram for the receiver of the proposed system

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Fig. 6: Details of block despreading procedure for user 1



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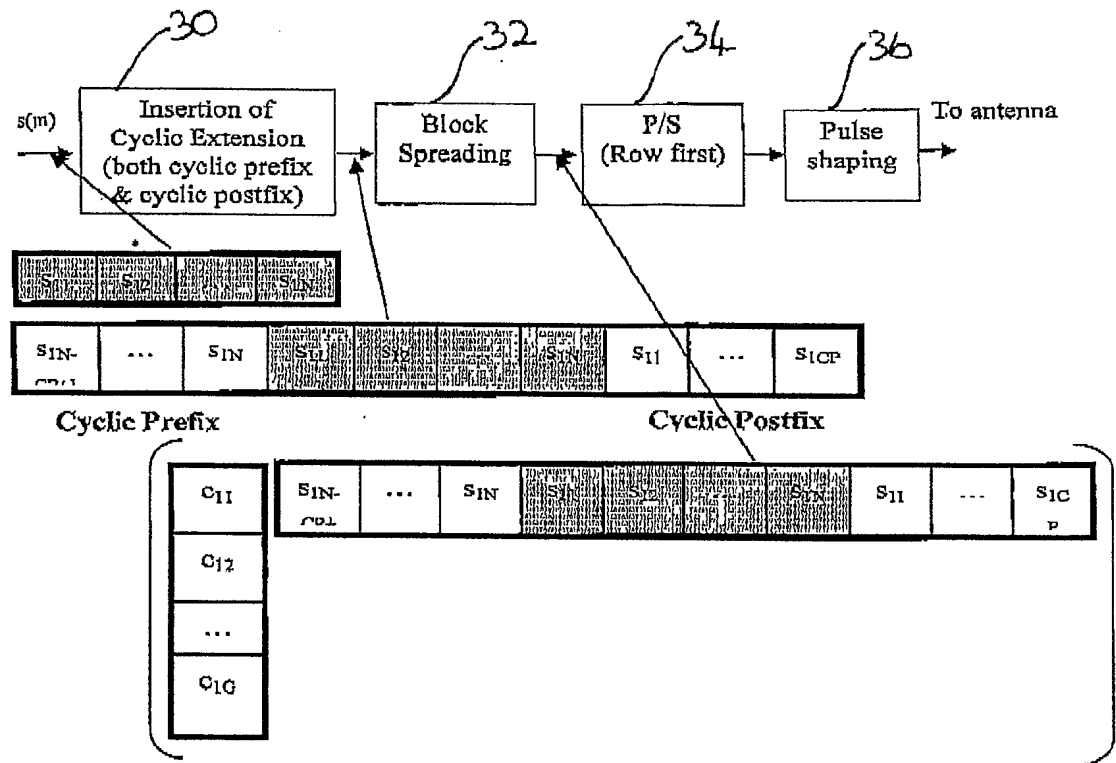
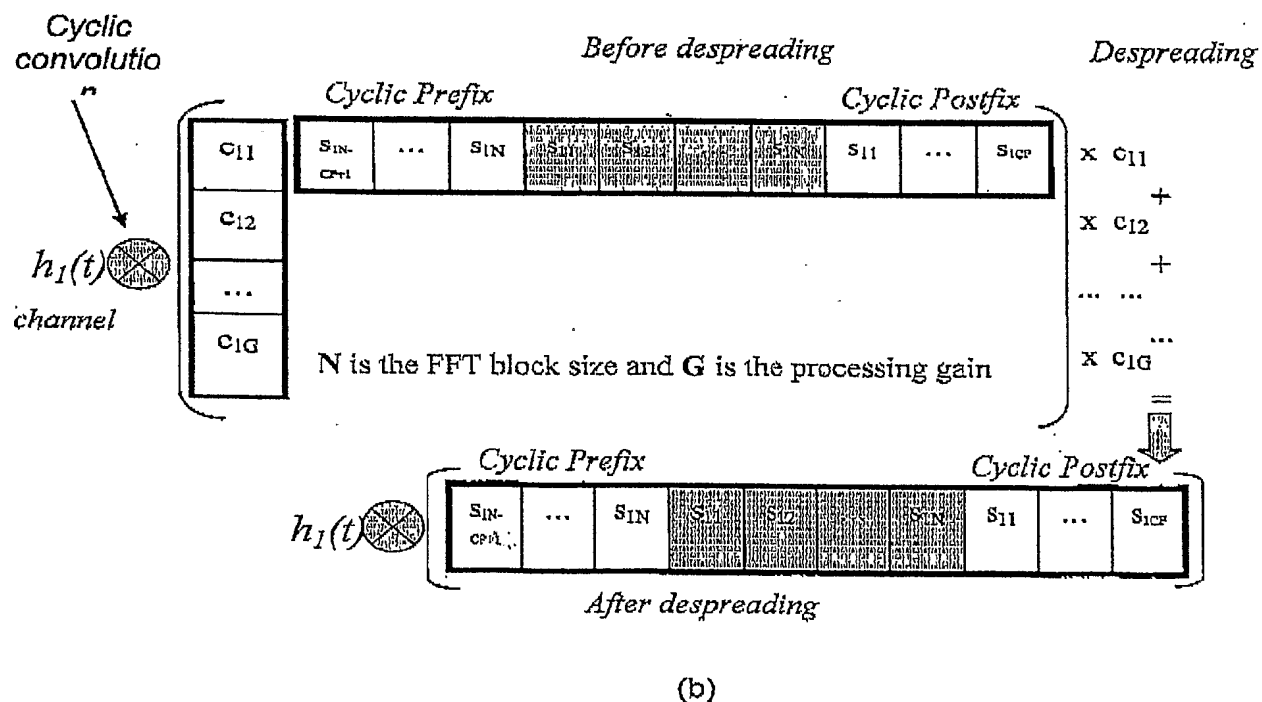
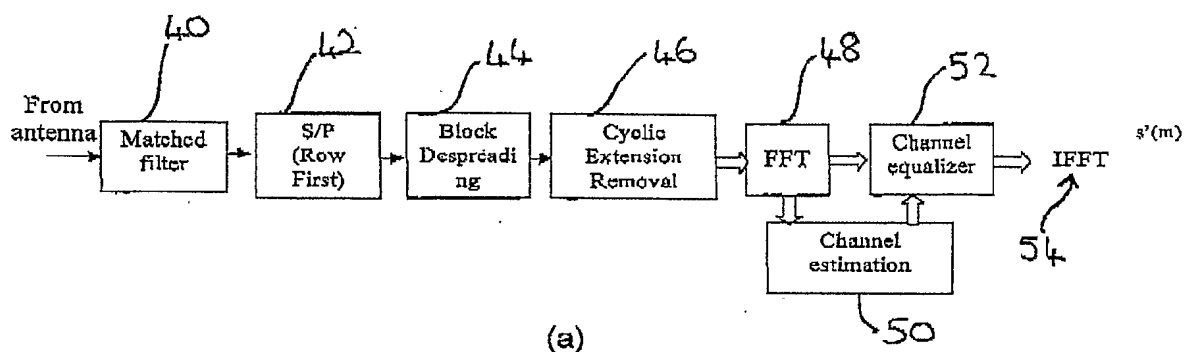


Fig. 7: Block diagram for the transmitter (Method 2)

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Fig. 8: Receiver structure for alternate method

- (a) Block diagram for the proposed receiver (alternate method)
 (b) Details of block despreading procedure



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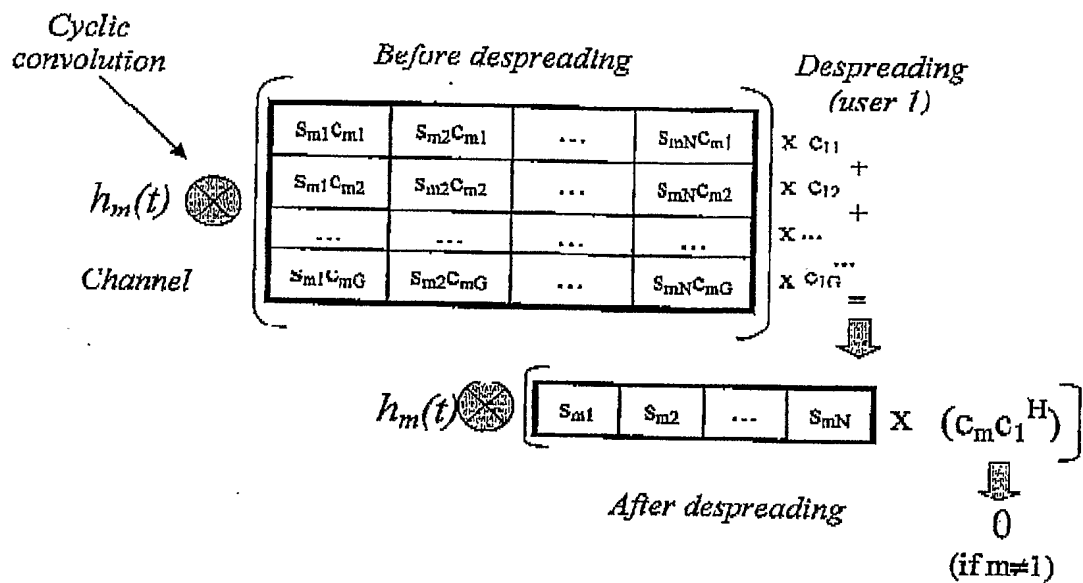


Fig. 9: Illustration on the effect of MAI for the proposed system

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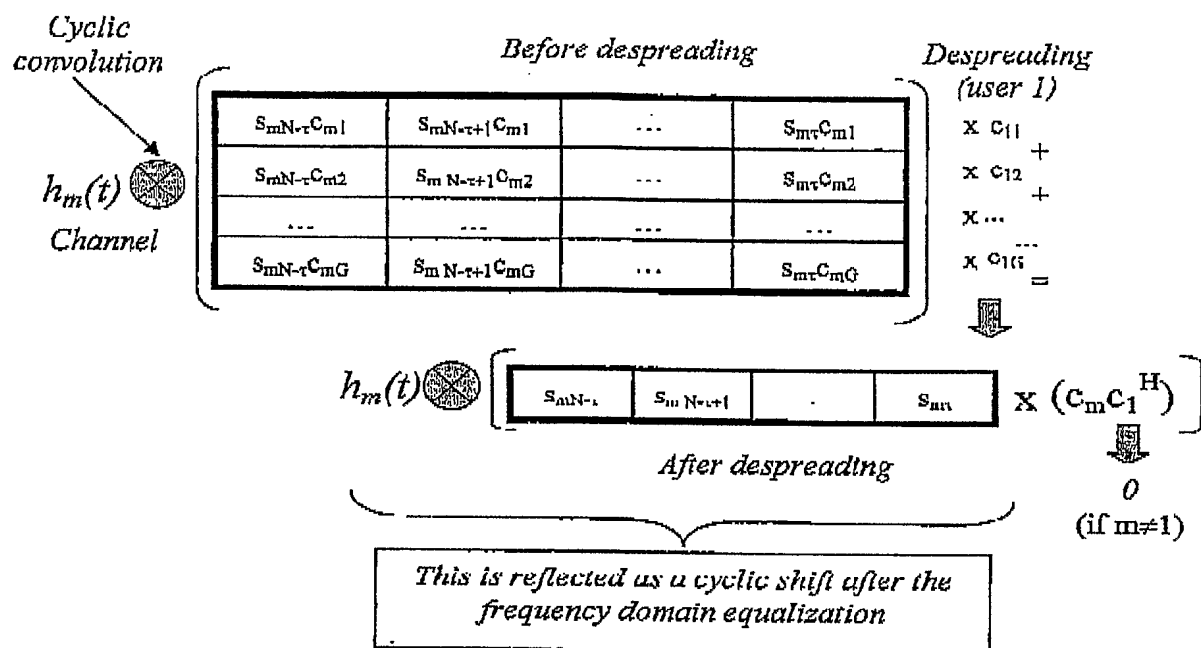


Fig. 10: Illustration on the effect of MAI when the users are asynchronous

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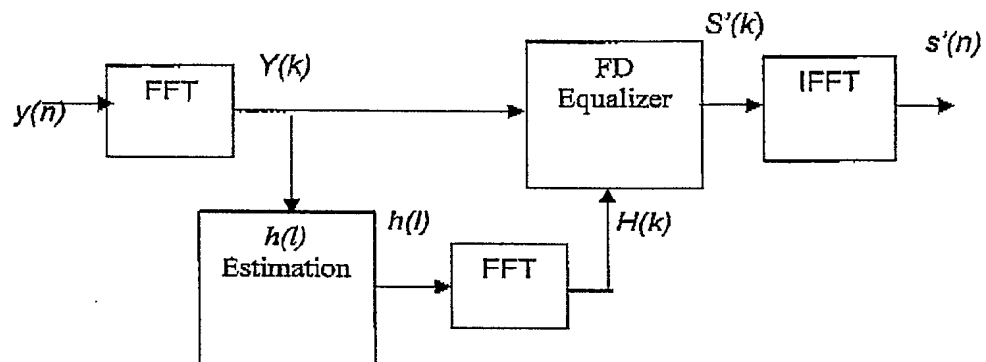


Fig. 11: Block diagram for the time-domain channel response estimation and frequency domain equalization

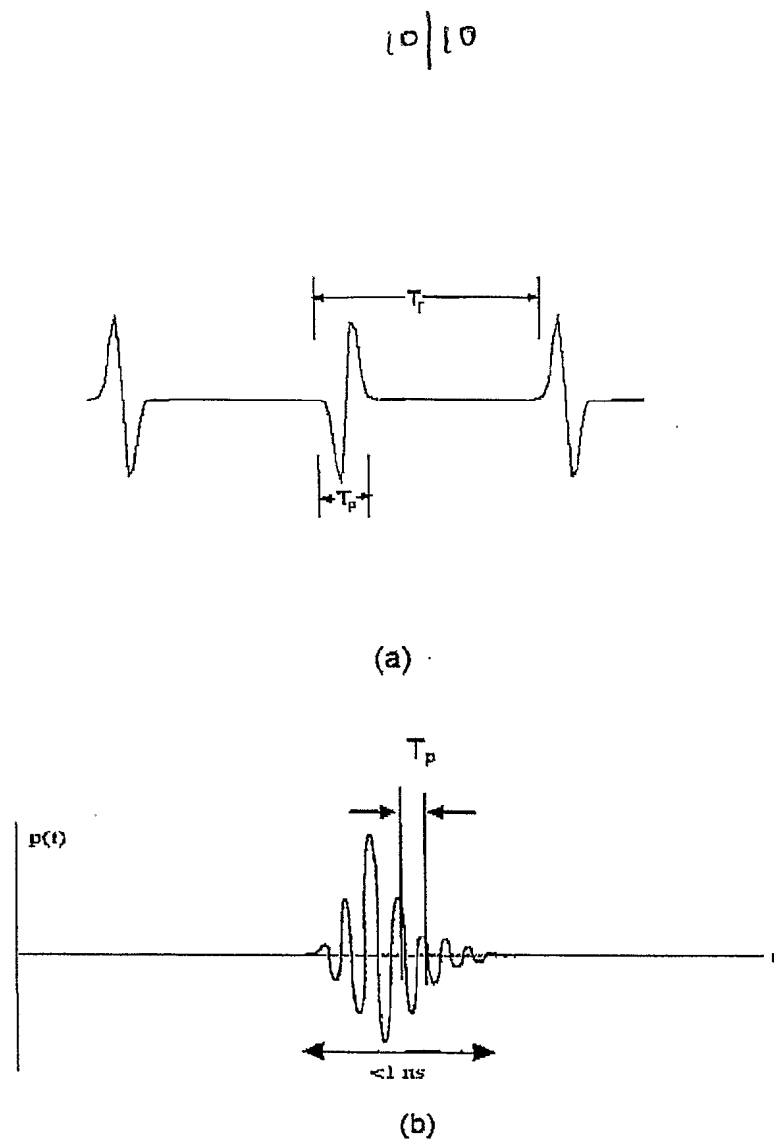


Fig. 12: Transmitted and received pulse shapes for ultra wideband transmission
 (a) Pulse shapes just before transmission, also shows the relation between pulse period (T_p), pulse repetition period (chip period) (T_r).
 (b) Typical received pulse for single pulse transmission without channel distortion